REMARKS

Applicant appreciates the Examiner's thorough consideration provided the present application. Claims 1-11 are now pending in the application. Reconsideration of the application in view of the remarks set forth below is respectfully requested.

Withdrawal of Objections and Rejections to the Claims

Applicant appreciatively notes that the Examiner's previous objection of claim 3, as well as the rejection of claims 1, 2, 5 and 8 under 35 U.S.C. § 112 have been withdrawn.

Claim Rejections Under 35 U.S.C § 103

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hashimoto (U.S. Patent No. 4,907,275) in view of Hasebe et al. (U.S. Patent No. 5,392,351, hereinafter "Hasebe") in further view of Yokota et al. (U.S. Patent No. 7,230,898, hereinafter "Yokota"); and claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hashimoto in view of Hasebe. These rejections are respectfully traversed.

For a 35 U.S.C. § 103 rejection to be proper, a prima facie case of obviousness must be established. See M.P.E.P. 2142. One requirement to establish prima facie case of obviousness is that the prior art references, when combined, must teach or suggest all claim limitations. See M.P.E.P. 2142; M.P.E.P. 706.02(j). Thus, if the cited references fail to teach or suggest one or more elements, then the rejection is improper and must be withdrawn.

Independent claim 1 recites, *inter alia*,

> "wherein when the digital recording signal needs to be encrypted, the encryption circuit begins to start up and the digital recording signal is transmitted from the data control circuit to the memory to be stored in the memory **during start-up of the encryption circuit**, and when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in the recording unit."

Hashimoto describes an encryption apparatus including an input buffer 14, an encryption processor 15 and an out put buffer 16. A plain text block sequence is input into input buffer 14.

The encryption processor 15 encrypts the plain text block sequence one block at a time and stores it into the output buffer 16. The plain text blocks not to be encrypted are sequentially read from the input buffer in the ascending order of the addresses and they are stored, without being encrypted, in the output buffer at the corresponding addresses to the input buffer addresses at which the plain text blocks have been stored. See Abstract, lines 1-15 of column 3 and Figure 2B of Hashimoto.

However, Hashimoto does not disclose or suggest that when a digital recording signal needs to be encrypted, an encryption circuit begins to start up and the digital recording signal is transmitted from a data control circuit to a memory to be stored in the memory during start-up of the encryption circuit. Also, when the encryption circuit becomes capable of operation, the digital recording signal stored in the memory is transmitted via the data control circuit to the encryption circuit and is encrypted by the encryption circuit to be recorded in a recording unit as claimed.

The Examiner asserts that Hashimoto, in lines 1-15, col. 3, discloses or suggests the above-noted claimed feature. The Examiner also alleges that the purpose of a buffer is to store data after it is transferred but before it can be processed either due to the circuit not having completed start-up or is currently processing other data. However, such allegation is without merit.

First, the cited portion of Hashimoto merely describes an input buffer 14 to store a plain text block sequence. The encryption processor 15 encrypts the plain text block sequence one block at a time and stores it into the output buffer 16. However, Hashimoto is completely silent with respect to the process of a digital recording/reproduction signal **during the time period when an encryption/decryption circuit is starting up [enabling]**.

Furthermore, the mere disclosure of an input buffer in Hashimoto does not provide any support for an assertion that Hashimoto discloses a buffer for storing data before it can be processed due to the circuit not having completed start-up. Hashimoto is not concerned with respect to a buffer for the alleged purpose. In contrast, Hashimoto discloses an input buffer for the purpose of encrypting the data one block at a time to ensure a sequential processing. See lines

1-15, col. 3 of Hashimoto. Thus, the Examiner appears to mischaracterize Hashimoto in an effort to satisfy the claimed features.

In addition, with the arrangement of claimed features, a recording/reproducing unit enables an encryption/decryption circuit only when encryption/decryption is required without interrupting recording/reproducing. Specifically, data can be continuously recorded/reproduced during a period of time from a time when a program that does not need to be encrypted/decrypted is switched to a program that needs to be encrypted/decrypted to a time when the recording/reproducing unit is ready to record/reproduce an encrypted/decrypted signal. As a result, a digital signal can be recorded or reproduced during start-up of an encryption circuit or decryption circuit.

Hashimoto is not concerned with providing such features. Thus, the Examiner's reasoning for supporting the allegation appears to be based on impermissible hindsight. See MPEP 2141. Thus, if this rejection is maintained, Applicant respectfully requests that the Examiner clearly identify prior art that allegedly teaches the claimed features.

Hasebe and Yokota do not remedy the deficiencies of Hashimoto.

Independent claim 2 recites, *inter alia*,

> "wherein when the digital recording signal encrypted and recorded on the recording medium needs to be decrypted and reproduced, during start-up of the decryption circuit, the digital recording signal having been stored before start-up of the decryption circuit is outputted via the data control circuit, and when the decryption circuit is capable of operation, the digital recording signal read by the reproducing unit is transmitted via the data control circuit to the decryption circuit and is decrypted by the decryption circuit to be outputted."

Independent claim 4 recites, *inter alia*,

> "a control unit which controls the storage unit and the encryption unit in such a way that when the determination unit determines that the digital signal does not need to be encrypted, the digital signal is not encrypted by the encryption unit and the digital signal stored in the storage unit is outputted, and when the determination unit determines that the digital signal needs to be encrypted, the digital signal from a time of the determination to a time when the enabling of the encryption unit is completed by the encryption key is stored in the storage unit and is encrypted by the encryption circuit to be outputted after the enabling of the encryption unit is completed."

Independent claim 7 recites, *inter alia*,

"a control unit which controls the storage unit and the decryption unit in such a way that when the determination unit determines that the digital signal does not need to be decrypted, the digital signal is not decrypted by the decryption unit and the digital signal stored in the storage unit is outputted, and when the determination unit determines that the digital signal needs to be decrypted, the digital signal from a time of the determination to a time when the enabling of the decryption unit is completed by the encryption key is stored in the storage unit and is decrypted by the decryption circuit to be outputted after the enabling of the decryption unit is completed."

Independent claim 10 recites, *inter alia*,

"wherein when the determination is that the digital signal does not need to be encrypted, the digital signal is not encrypted and the stored digital signal is outputted, and when the determination is that the digital signal needs to be encrypted, the digital signal from a time of the determination to a time when the function of encrypting is enabled is stored and is encrypted to be outputted after the enabling of the function of encrypting is completed."

Independent claim 11 recites, *inter alia*,

"wherein when the determination is that the digital signal does not need to be decrypted, the digital signal is not decrypted and the stored digital signal is outputted, and when the determination is that the digital signal needs to be decrypted, the digital signal from a time of the determination to a time when the function of decrypting is enabled is stored and is decrypted to be outputted after the enabling of the function of decrypting is completed."

In view of the above remarks, Applicant respectfully submits that the grounds of rejection set forth in the Office Action fails to establish that the prior art teaches a process of a digital recording/reproduction signal **during the time period when an encryption/decryption circuit is starting up [enabling]**. Consequently, the rejection fails to establish prima facie obviousness of any of the rejected claims. Thus, Applicant respectfully requests reconsideration withdrawal of the Examiner's rejection under 35 USC § 103.

CONCLUSION

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Dennis P. Chen, Reg. No. 61,767, at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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